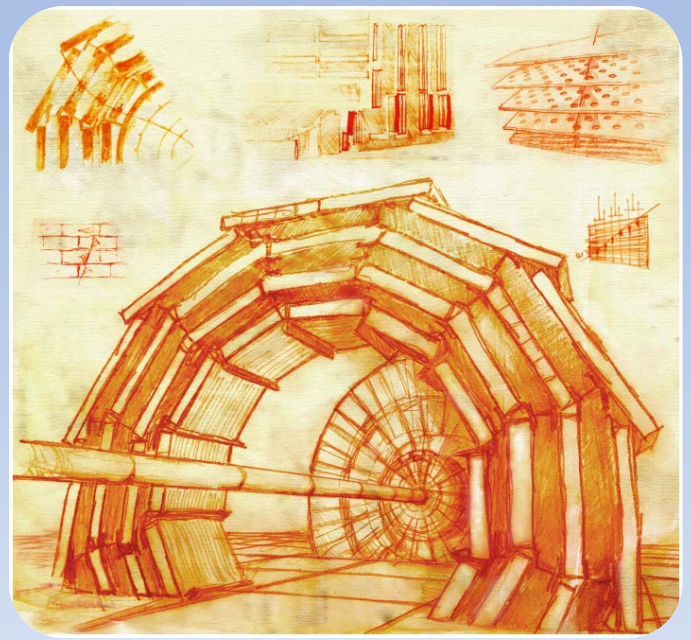
Phase-II Upgrade of Link Board System

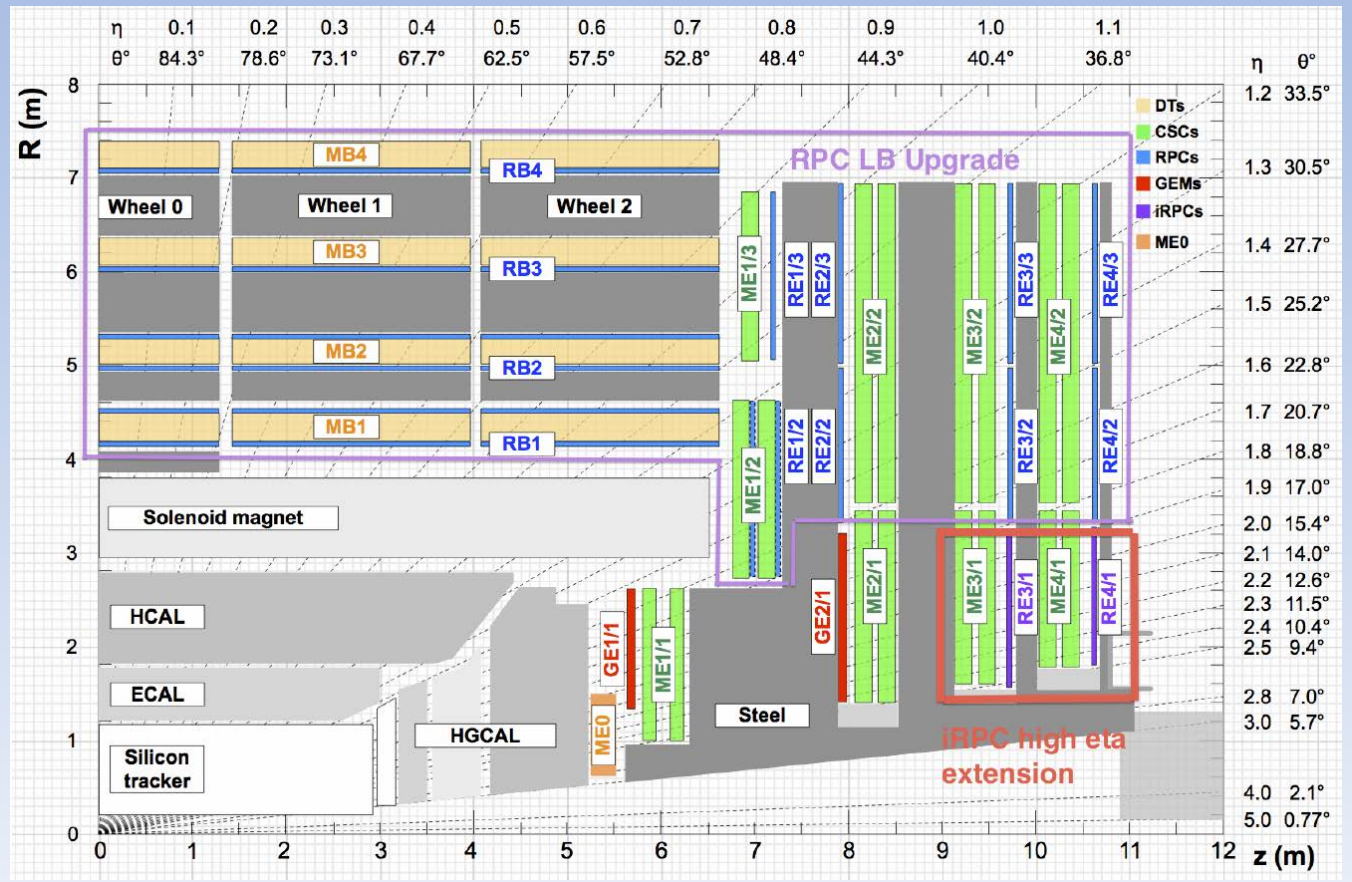


Behzad Boghrati
on behalf of the IPM & CMS Collaboration
26th October 2017

IPM-CMS Lab colleagues

- **Ahmad Ramezani**, Amir Kabir University (Tehran Polytechnics) , Project Consular and Software Programmer
- **Mohammad Ebrahimi**, University of Tehran, Mitigation of Radiation Effects on FPGAs
- **Vaheed Amozegar**, Sharif University, RPC Syncoder and the Timing systems
- **Haniyeh Ghasemi**, Amir Kabir University (Tehran Polytechnics), Computer Hardware Designer, Giga bit Data transmission

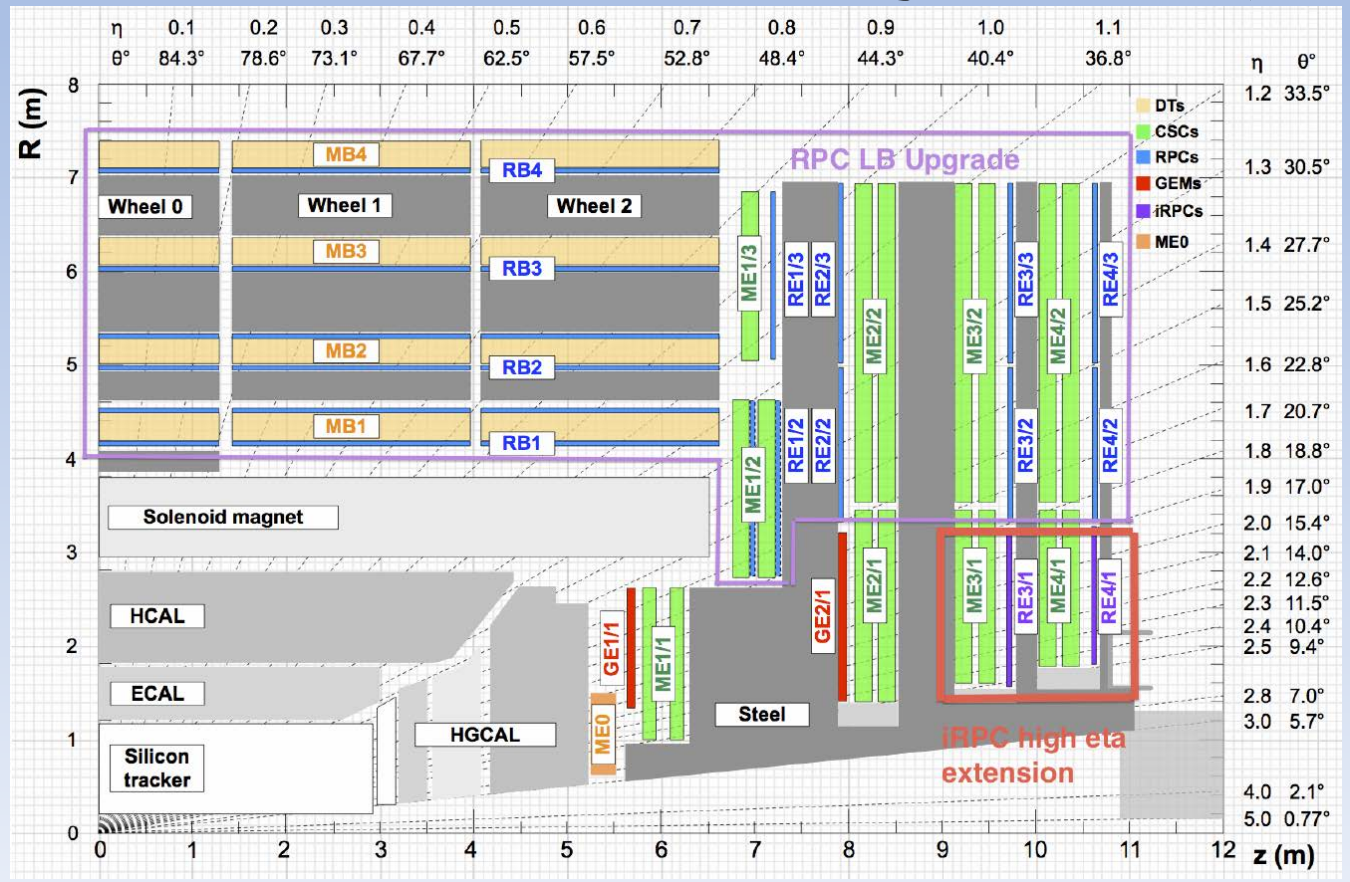
Overview of the RPC upgrades



Two important upgrades are planned:

- the RPC off-detector readout electronics (called link system) will be replaced because :
  - New link system improves timing resolution from 25 ns to 1.6 ns
  - Maintenance of old Link board system is very not possible
  - Radiation effects and Aging
- the RPC coverage will be extended from $|\eta|$ = 1.9 up to 2.4.

Properties of the CMS Muon system (2016)

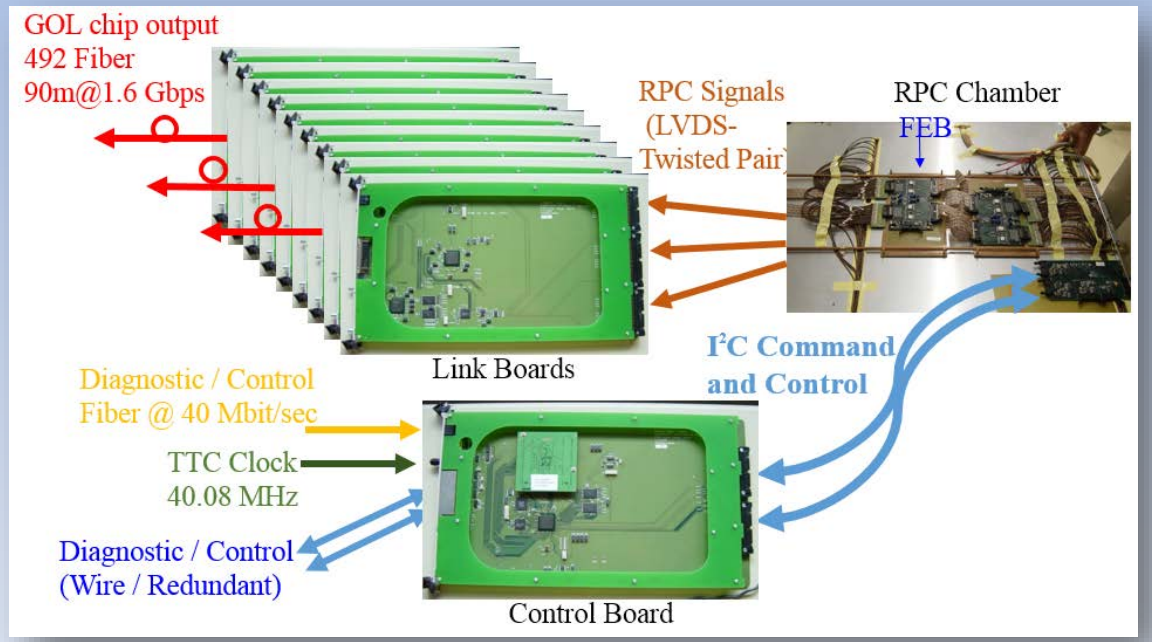


Muon subsystem	Drift Tubes (DT)	Cathode Strip Chambers (CSC)	Resistive Plate Chambers (RPC)
$\|\eta\|$ range	0.0–1.2	0.9–2.4	0.0–1.9
Number of chambers	250	540	Barrel 480 Endcap 576
Number of layers/station	r-ϕ: 8; z: 4	6	2 in RB1 and RB2 1 elsewhere
Surface area of all layers	18 000 m^2	7000 m^2	Barrel 2300 m^2 Endcap 900 m^2
Number of channels	172 000	Strips 266 112 Anodes 210 816	Barrel 68 136 Endcap 55 296
Spatial resolution	100 μm	50 – 140 μm	0.8 – 1.3 cm
Time resolution	2 ns	3 ns	1.5 ns*
Fraction of working channels	98.4%	99.0%	98.3%

Structure of Current RPC Readout System

Front End Boards – on chambers

Discriminates the analogue strip signals (applies programmable threshold) and forms them into **digital pulses** in the LVDS standard. The **rising edge** of the output pulse defines the time of the chamber hit.
Control and monitoring: I2C (the I2C controller is CB)



Link Box – off detector / balconies

- **Link Boards** (up to 18 per Link Box)
  Receive the signals from the chambers (one LB = one chamber/roll), 96 input channels=strips, **synchronize** the signals, compress and send them through the optical links to the trigger processors **(OMTF, EMTF/CPPF, TwinMux + legacy Trigger Boards PAC).**
- **Control Boards** (2 per Link Box)
  Crate controller, contains CCU chip, 12 CBs forms FEC Chain or token rings. **Controls the FEBs via I2C**
- **Backplane**
  The LV cables, the signal cables from chambers and the I2C cables are connected to it.
- **Frontples** (2 per Link Box)
  provides communication between the CBs and LBs, and between the Slave and Master LBs

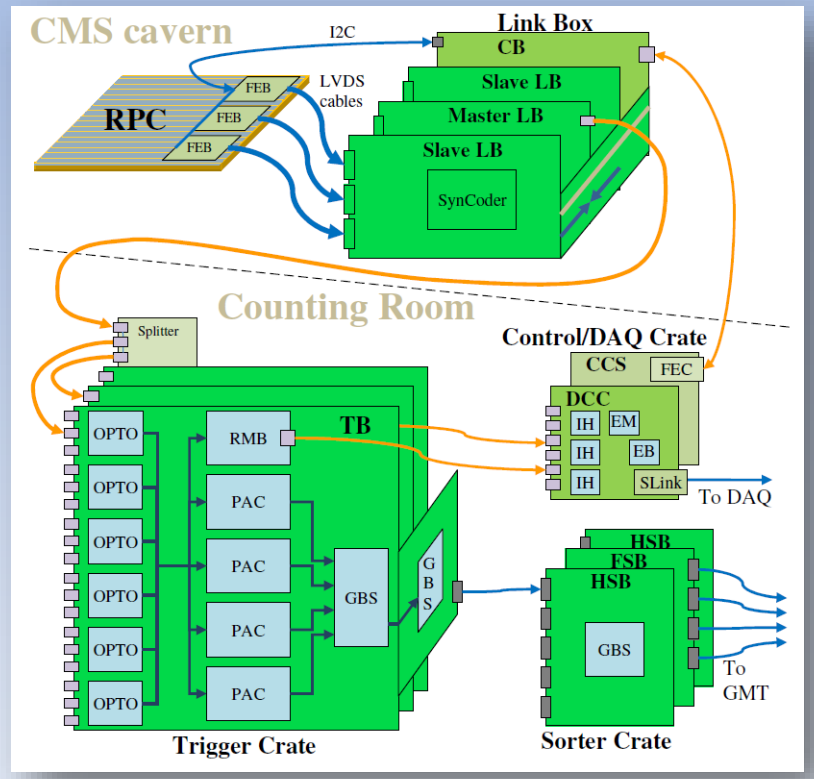
Structure of Current RPC Readout System

Front End Boards – on chambers

Discriminates the analogue strip signals (applies programmable threshold) and forms them into **digital pulses** in the LVDS standard. The **rising edge** of the output pulse defines the time of the chamber hit.
Control and monitoring: I2C (the I2C controller is CB)

Link Box – off detector / balconies

- **Link Boards** (up to 18 per Link Box)
  Receive the signals from the chambers (one LB = one chamber/roll), 96 input channels=strips, **synchronize** the signals, compress and send them through the optical links to the trigger processors **(OMTF, EMTF/CPPF, TwinMux + legacy Trigger Boards PAC).**
- **Control Boards** (2 per Link Box)
  Crate controller, contains CCU chip, 12 CBs forms FEC Chain or token rings. **Controls the FEBs via I2C**
- **Backplane**
  The LV cables, the signal cables from chambers and the I2C cables are connected to it.
- **Frontples** (2 per Link Box)
  provides communication between the CBs and LBs, and between the Slave and Master LBs



CCS/FEC boards – communication channel

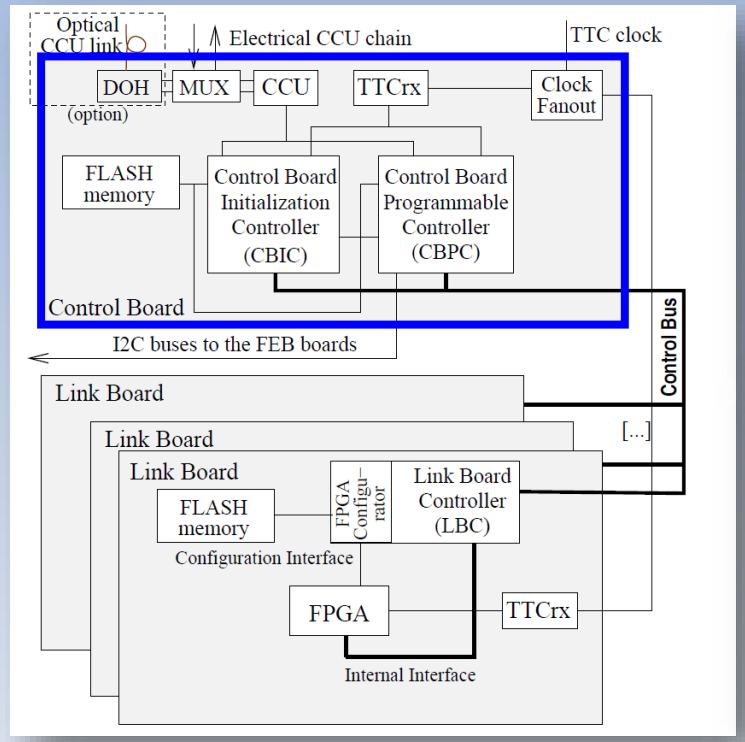
3 CCS boards (in VME crate in in the USC), each CCS contains 8 FEC mezzanine.

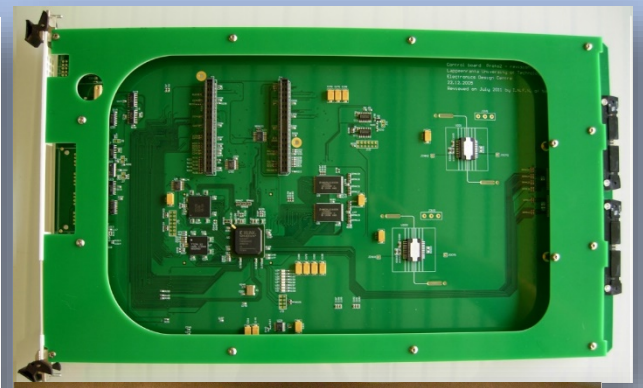
The Current Control Board (CB)

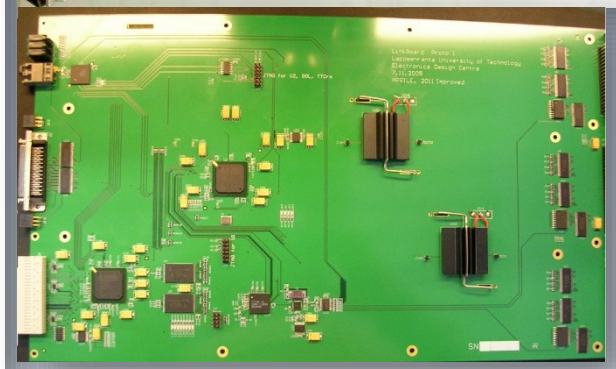
- Communication with the managing host (XDAQ or proprietary software)
- Transmission of the control and diagnostic data to and from the Front End Boards
- Transmission of the control and diagnostic data to and from the Link Boards
- Refreshing of the configuration of the programmable FPGA chips

Problems to be NOTICE in CB system

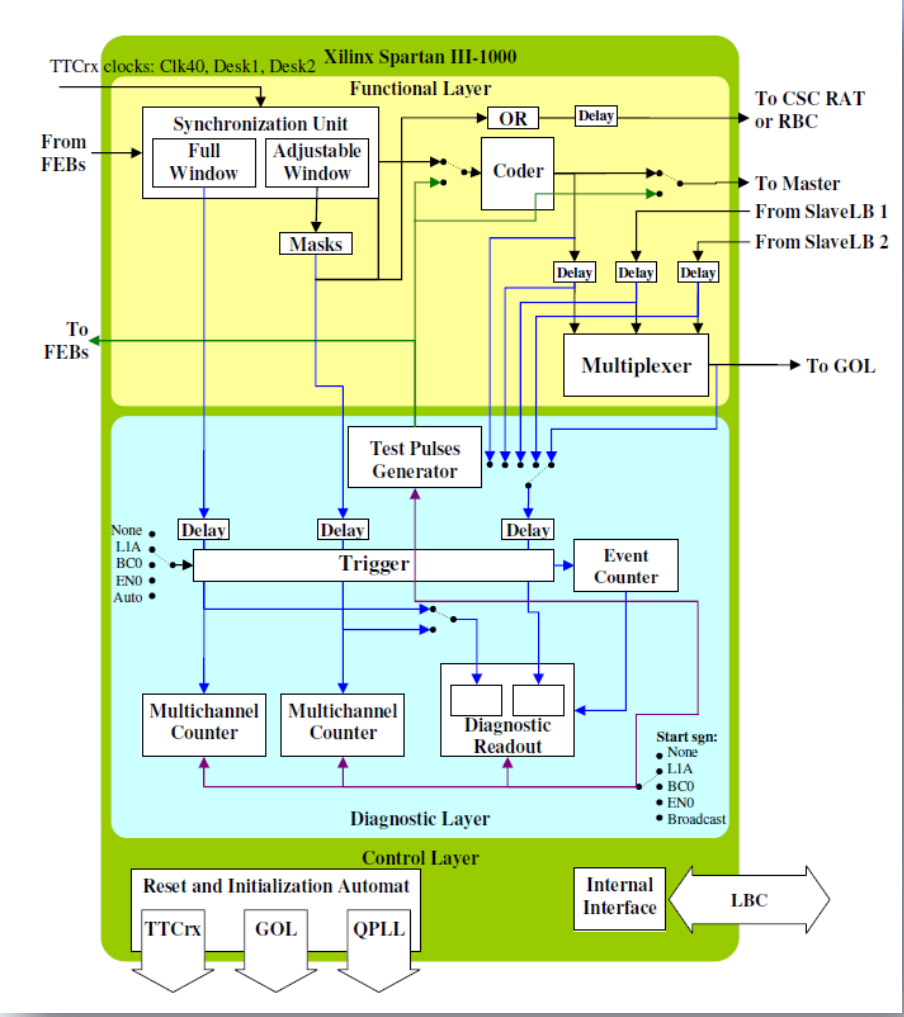
- High reliability of the system .Its failure renders part of the link system unusable
- Two contradictory requirements
- Keeping costs as low as possible

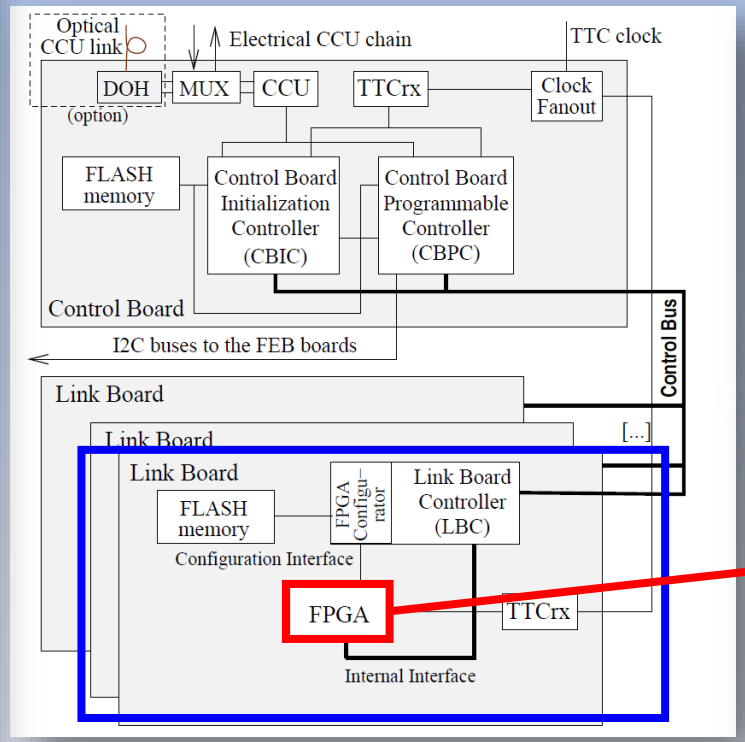


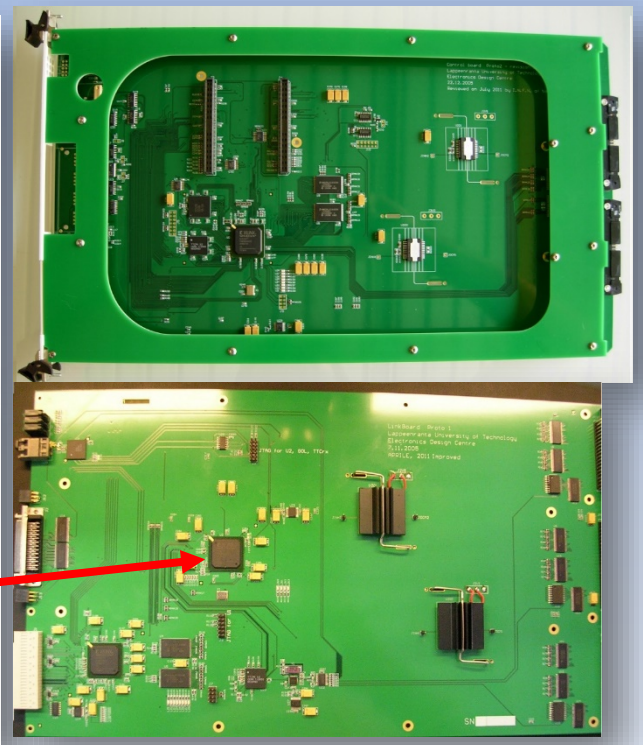




The Current Link Board (LB)

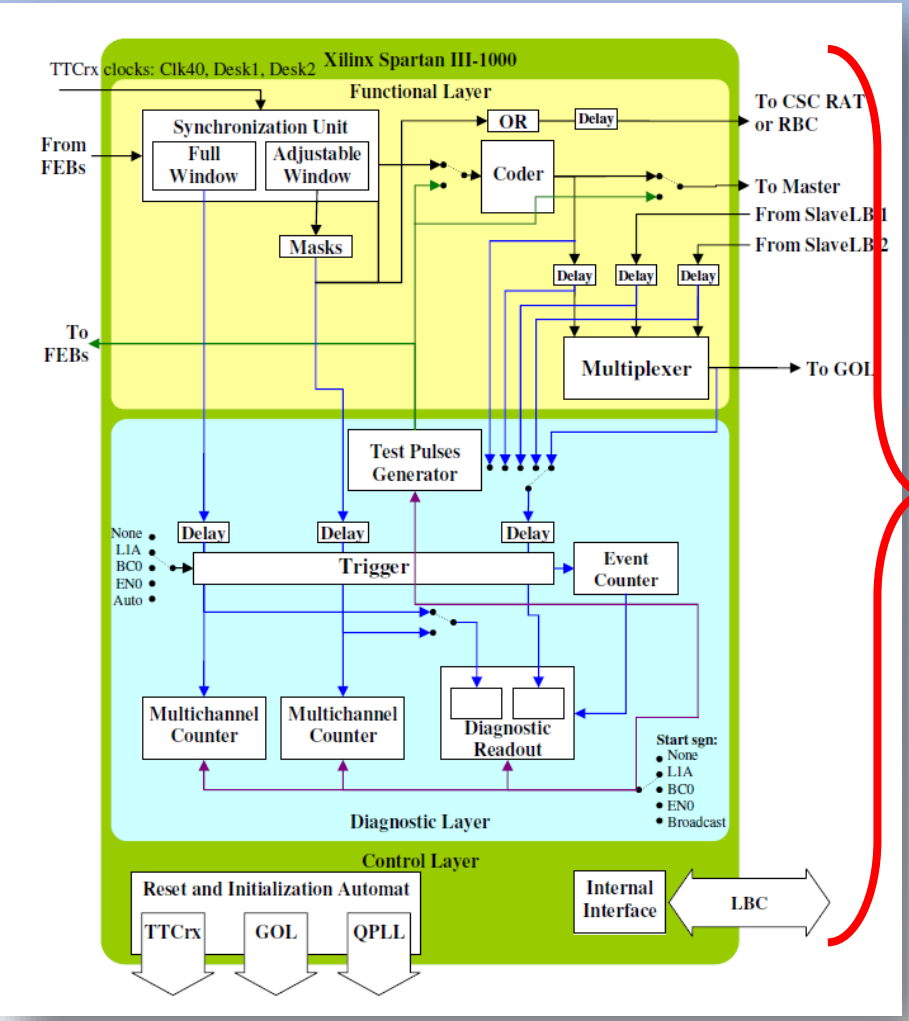


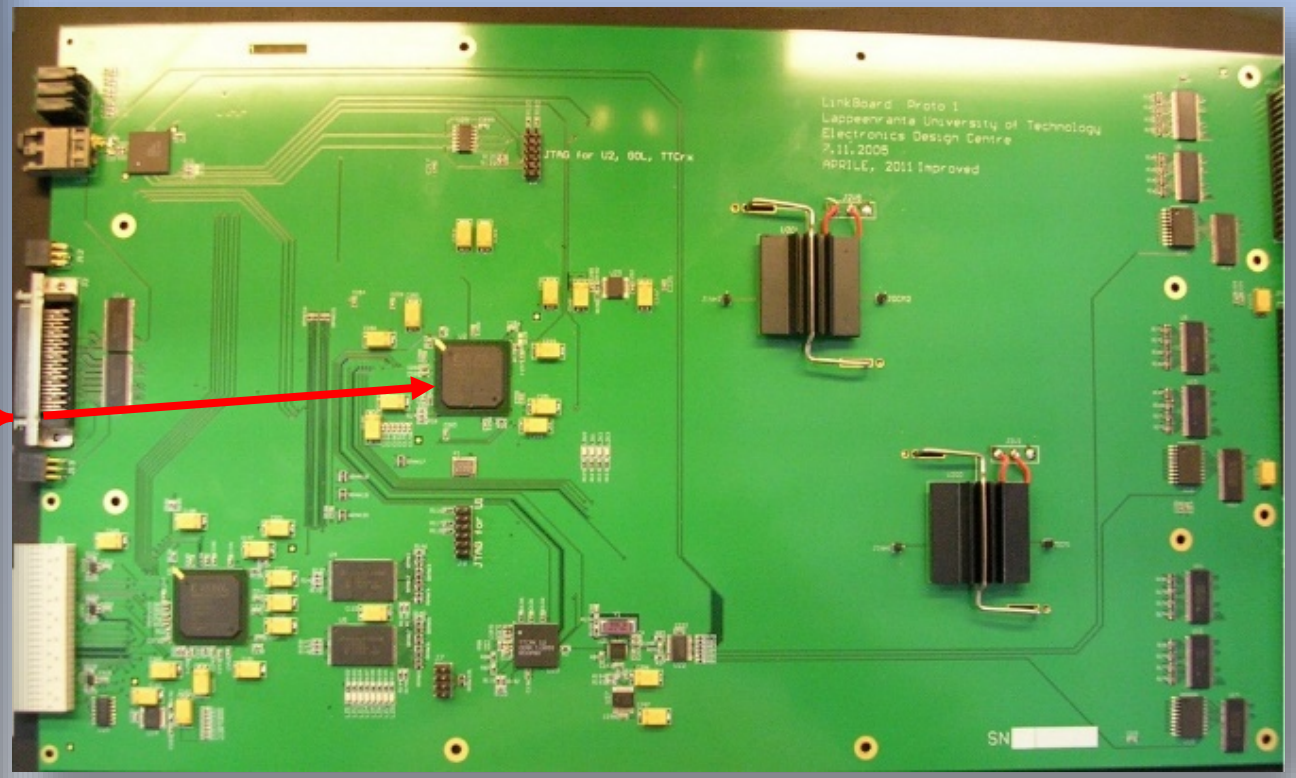




The Link Board SynCoder Device (FPGA) functional scheme

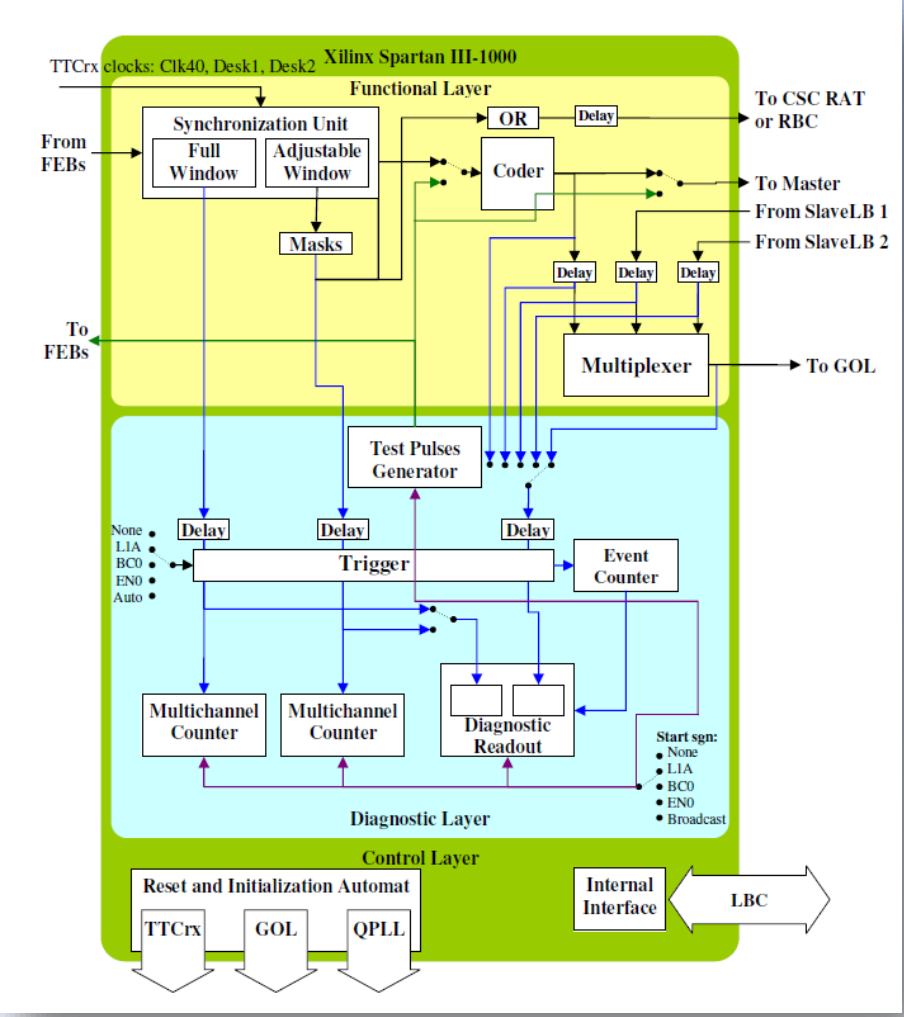
The Link Board SynCoder

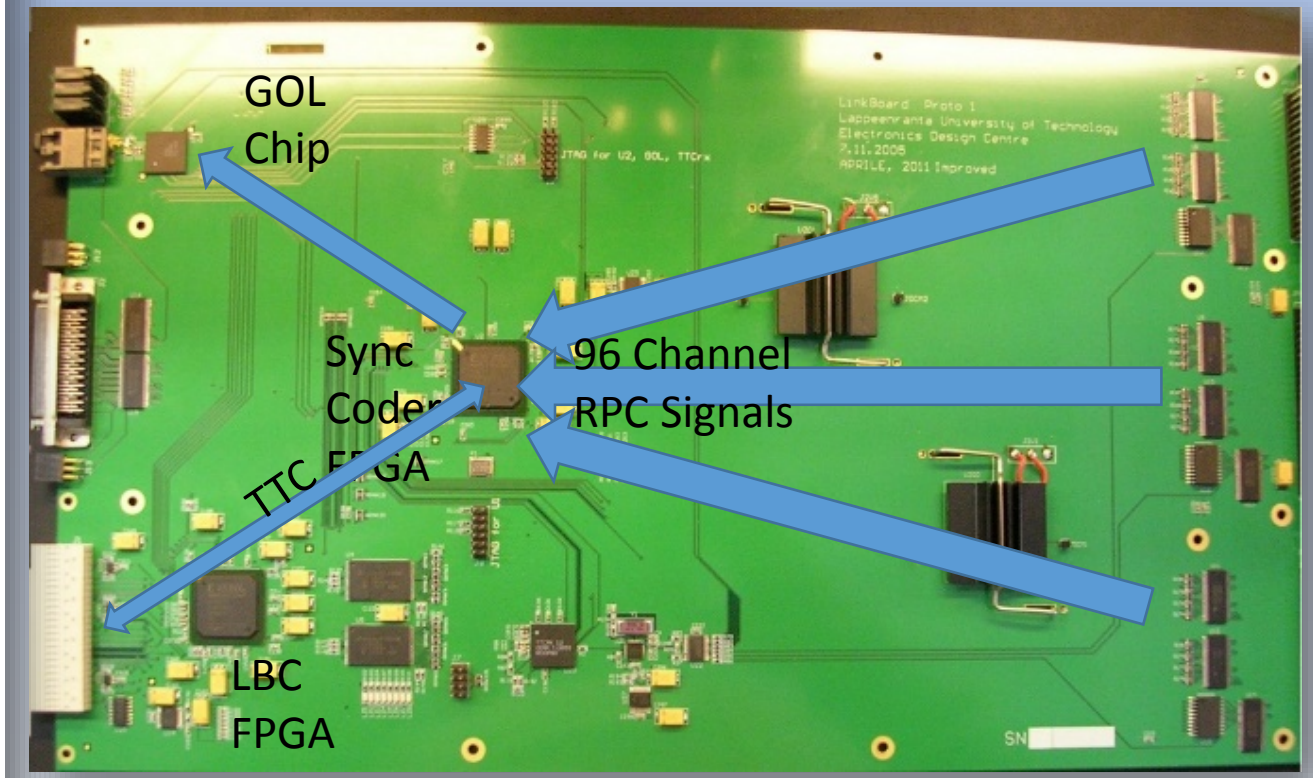




The Link Board SynCoder Device (FPGA) functional scheme

The Link Board SynCoder

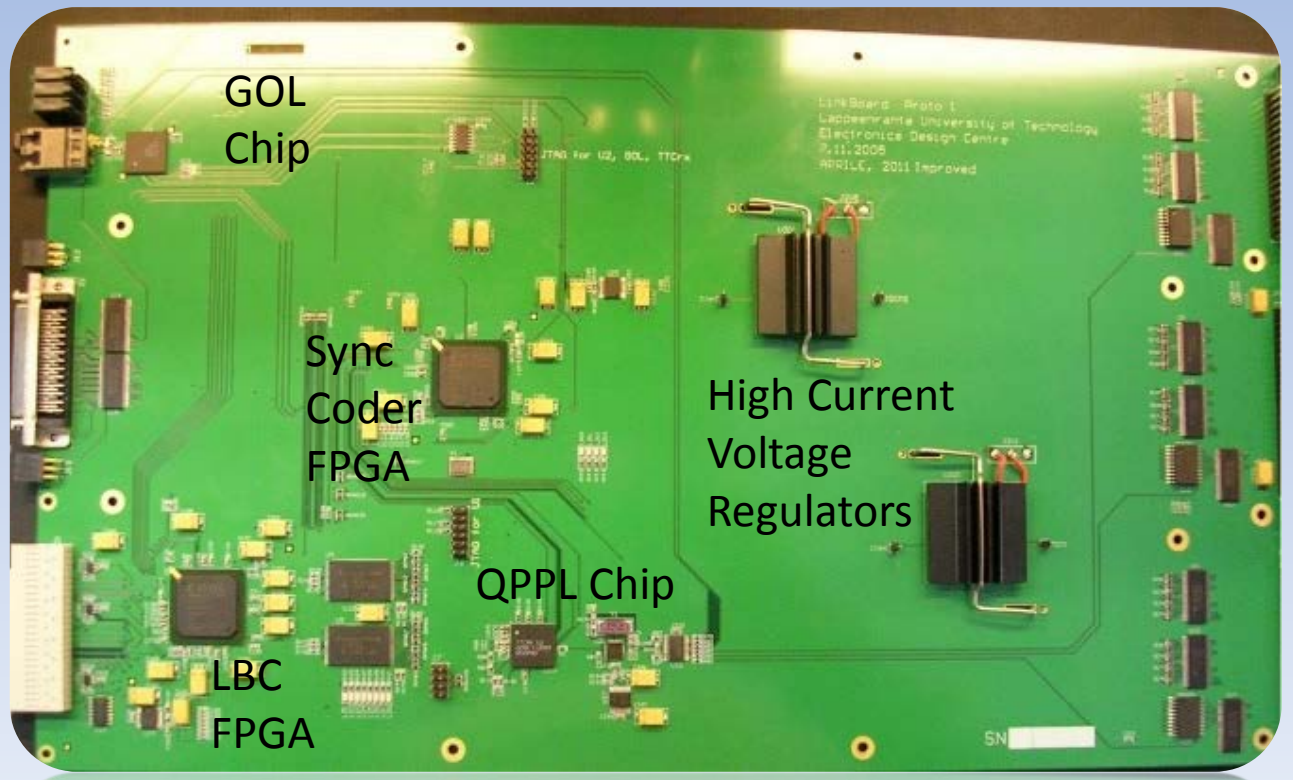




The Link Board SynCoder Device (FPGA) functional scheme

What sections must be changes

- The FPGAs Should be replaced with new version, larger digital resources
- GOL chips is obsolete and should be replaced with the other Giga bit optical interface
- The QPLL is obsolete too and should be implemented into the FPGA
- The High current Regulators should be replaced the new versions

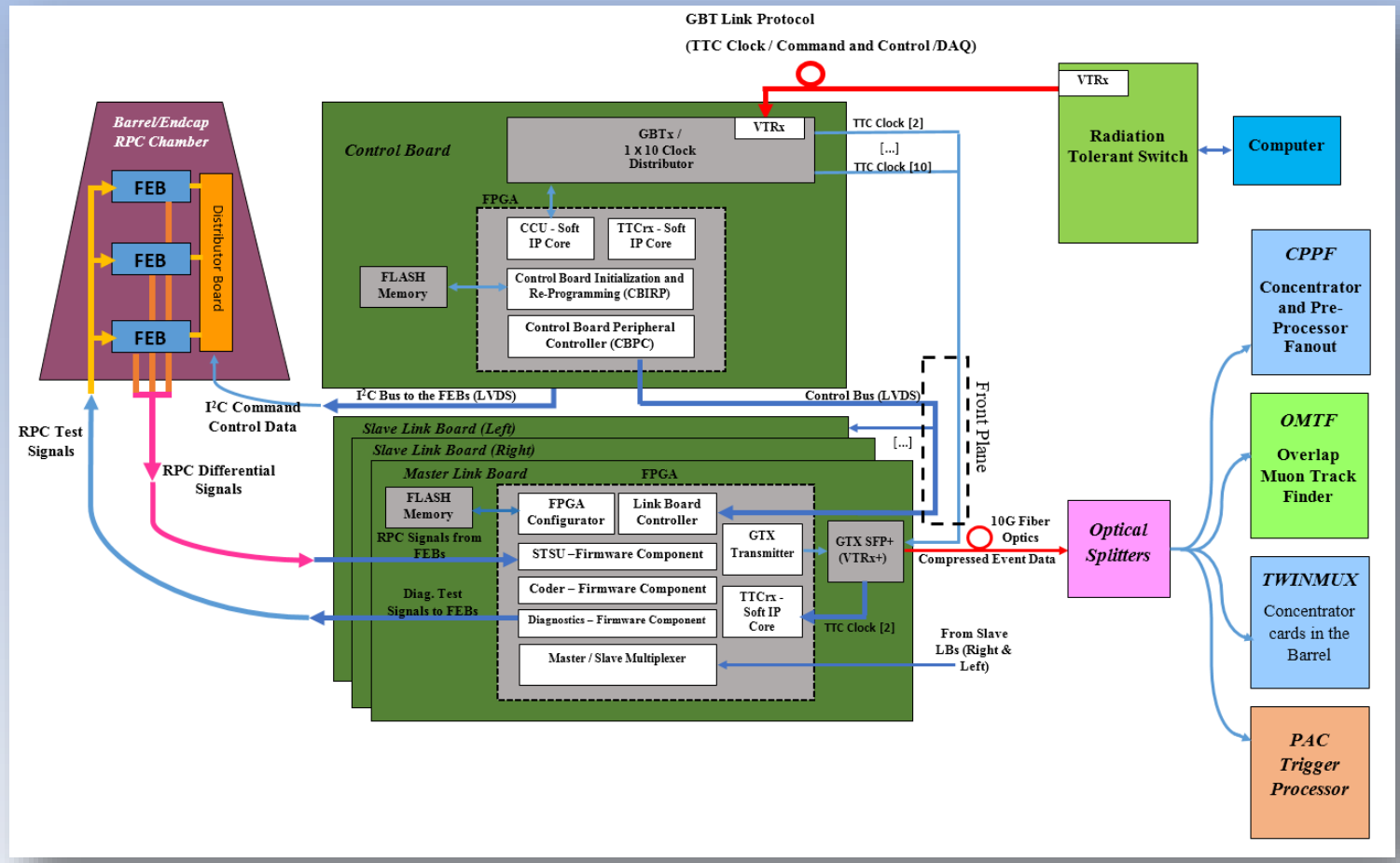


Current Link system other issues

- Spare Boards Availability
- Compatibility of “Standard” and “RE4 versions”
- Electronics Aging
- Radiation Exposure
- The rate of RPC Signal in HL-LHC
- Fastness of The FEC/CCU Configuration time and the Monitoring process
- EMI and CCU
- Link boards Firmwares

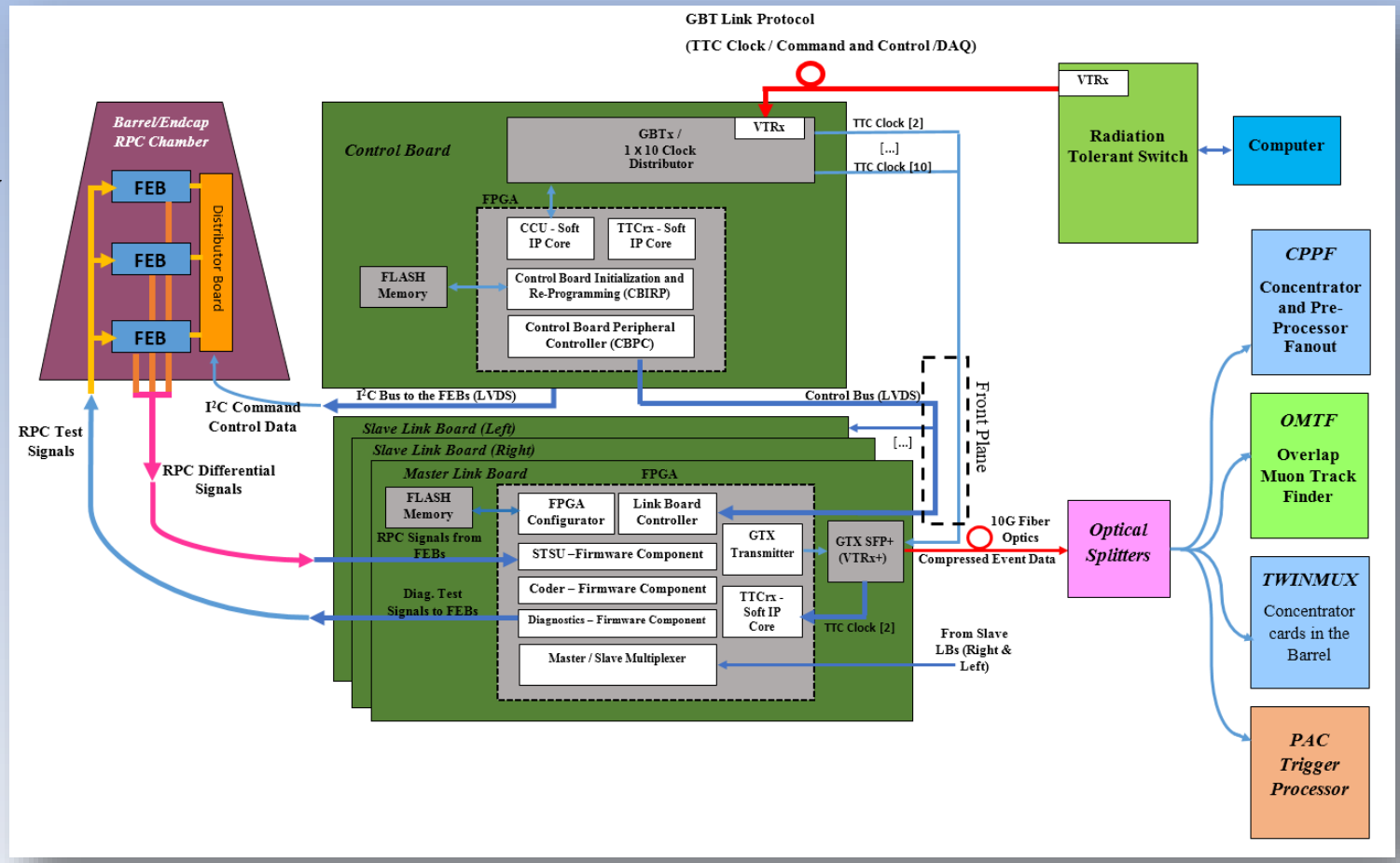
What we are going to do in Upgrade Phase-II – Control Board

- New Version of Control board
- New 7 series of Xilinx FPGA chips
- Radiation Hard GBT architecture
- GBTX , GBT-FGPA, VTRx optical converter (1310 nm) at higher speeds of 4.8 Gbps
- Improved the EMI and EMC
- Radiation tolerant FLASH-Based Smart Fusion family of Micro semi FPGA
- External Scrubber
- Reliable Remote Control and Programming
- The Availability of the system



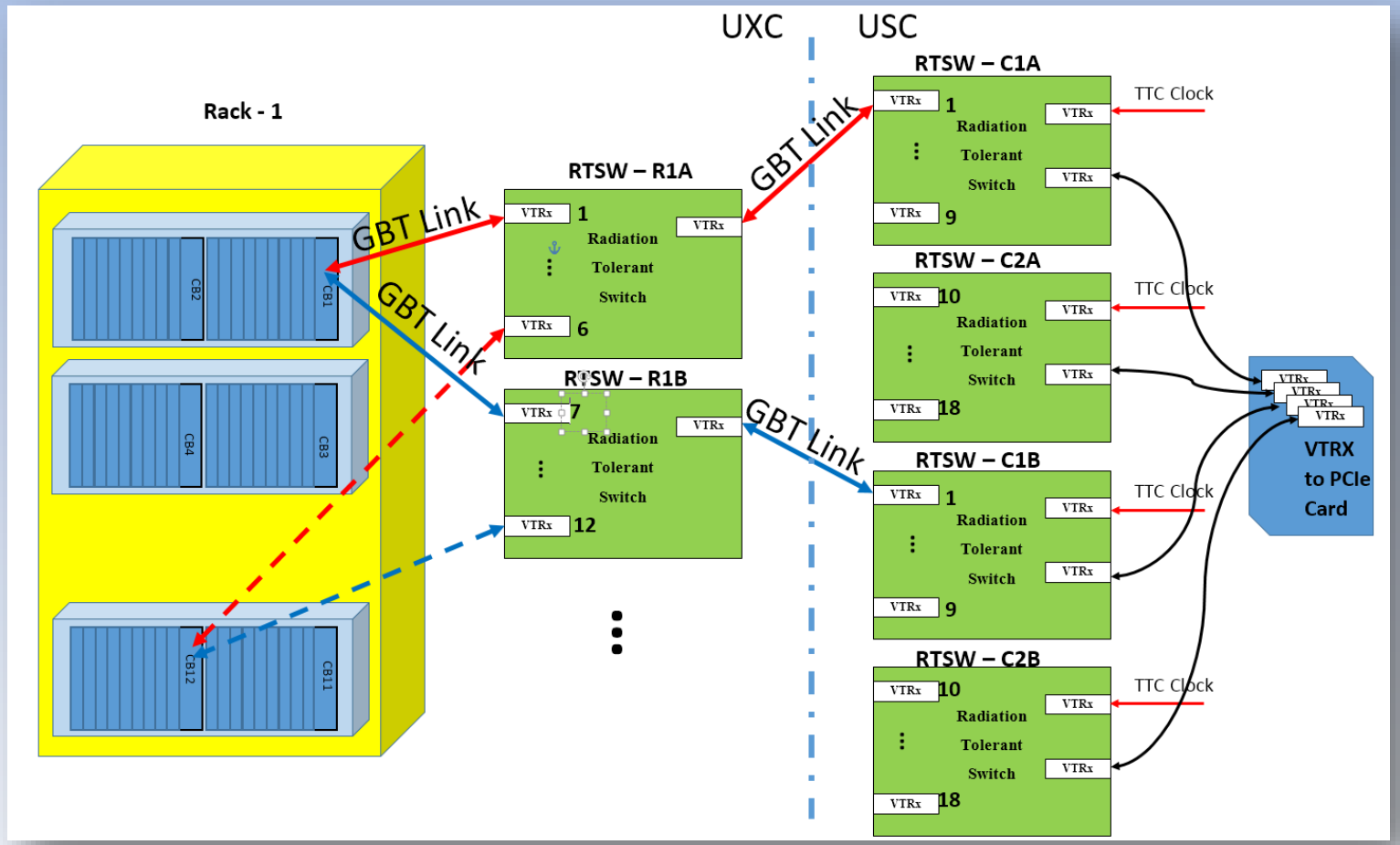
What we are going to do in Upgrade Phase-II – Link Board

- New Version of Link Boards
- New 7 series of Xilinx FPGA chips
- Dynamic Partial Reconfiguration, new techniques of Radiation Mitigations, SEM, ECC
- GTX , VTRx+ optical converter (1310 nm) at higher speeds of 10 Gbps
- Improved the EMI and EMC
- Radiation tolerant FLASH-Based Smart Fusion family of Micro semi FPGA
- External Scrubber
- Reliable Remote Control and Programming
- The Availability of the system



Upgrade Phase-II New Design- Communication and Control Chain

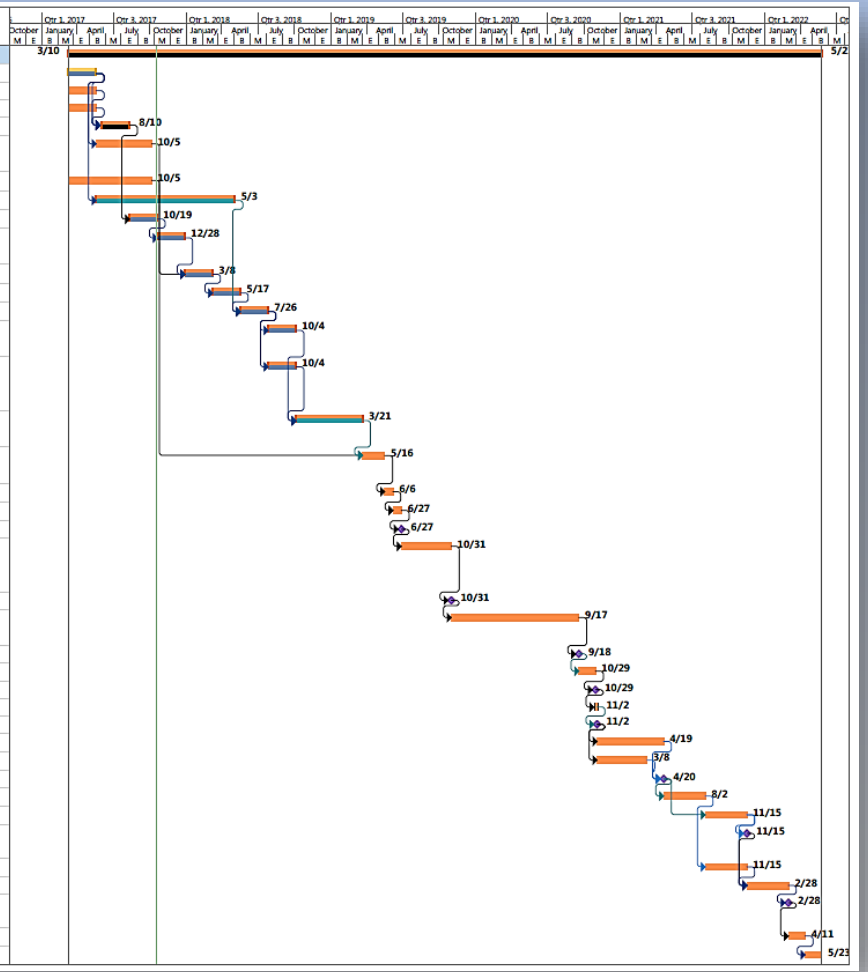
- Radiation Tolerant Redundant Switch
- New 7 series of Xilinx FPGA chips
- Dynamic Partial Reconfiguration, new techniques of Radiation Mitigations, SEM, ECC
- GTX , VTRx+ optical converter (1310 nm) at higher speeds of 10 Gbps
- Improved the EMI and EMC
- Radiation tolerant FLASH-Based Smart Fusion family of Micro semi FPGA
- External Scrubber
- Reliable Remote Control and Programming
- The Availability of the system



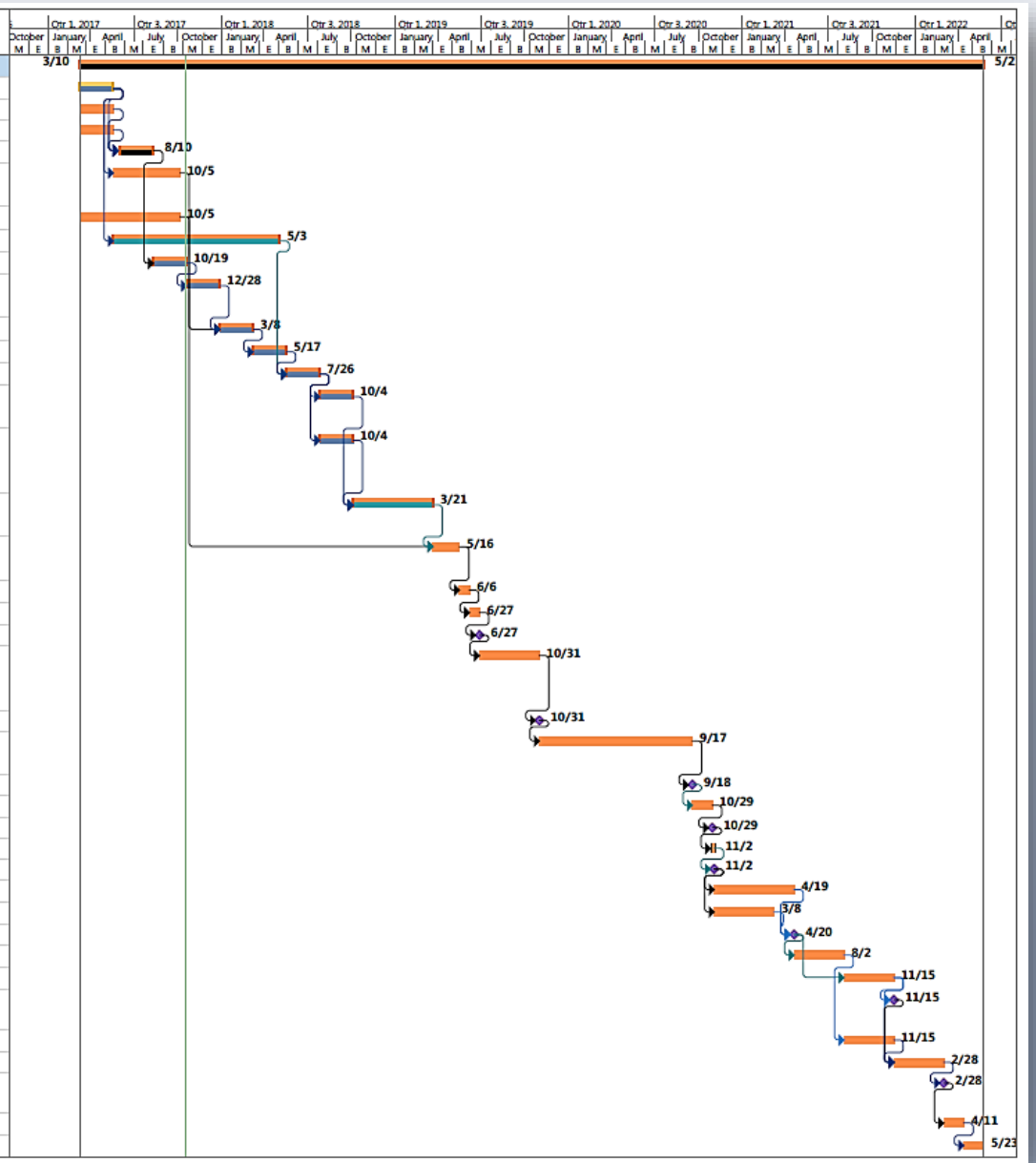
Link Board Upgrade Phase-II Time Schedule

- **Three main phases**
  - **Research and investigation**
  - **Design and Development of LB system prototype**
  - **Production**

ID	Task Name	Duration	Start	Finish
0	LinkBoard Final Gantt V1-A6_2017_08_03	271.4 wks	March 10, 2017	May 23, 2022
1	1 Analyzing the Legacy SCH & PCBs	10 wks	March 10, 2017	May 18, 2017
2	1.1 LinkBoard	50 days	March 10, 2017	May 18, 2017
3	1.2 Control Board	50 days	March 10, 2017	May 18, 2017
4	2 Analyzing the Legacy FPGA'S Firmware	10 wks	June 2, 2017	August 10, 2017
9	3 Analyzing the Communication Protocol (Reciever/ Transmitter)	100 days	May 19, 2017	October 5, 2017
10	4 FPGA Selection Study	150 days	March 10, 2017	October 5, 2017
11	5 Single Event Upset Study on FPGAs	50 wks	May 19, 2017	May 3, 2018
13	6 Analyzing of ASIC Chips	10 wks	August 11, 2017	October 19, 2017
20	7 Design and Simulation of ASIC Chip IP Cores by FPGAs	10 wks	October 20, 2017	December 28, 2017
27	8 Implementing of ASIC Chip IP Cores in FPGAs	10 wks	December 29, 2017	March 8, 2018
34	9 Hardware Test ot the IP Cores/ Re-Design	10 wks	March 9, 2018	May 17, 2018
41	10 Implementing of IP Cores in FPGAs +SEU	10 wks	May 18, 2018	July 26, 2018
48	11 Hardware Test of IP Cores in FPGAs + SEU with SEU Emulator / Re-Design	10 wks	July 27, 2018	October 4, 2018
55	12 Hardware Test of IP Cores in FPGAs + SEU with Proton Beam/fem Laser/Plasma Focus / Re-Design	10 wks	July 27, 2018	October 4, 2018
62	13 Integration of Cores and Design of Initial Prototype	24 wks	October 5, 2018	March 21, 2019
75	14 Prototype Test of Initial Linkboard/Control Board / Re-Design	40 days	March 22, 2019	May 16, 2019
76	15 Final Prototype Design / Documentation	15 days	May 17, 2019	June 6, 2019
77	16 Final Prototype Design Review / Documentation	15 days	June 7, 2019	June 27, 2019
78	17 Final Prototype Design Ready	0 days	June 27, 2019	June 27, 2019
79	18 Initial Validation (Hardware test of the chips +SEU with Proton beam/fem Laser/Plasma Focus/ Re-design)	90 days	June 28, 2019	October 31, 2019
80	19 Initiale Validation of Final Prototype in IPM	0 wks	October 31, 2019	October 31, 2019
81	20 Final Validation of Final Prototype Design at CERN	230 days	November 1, 2019	September 17, 2020
82	21 Final Validation of Final Prototype Design At CERN	0 days	September 18, 2020	September 18, 2020
83	22 Finalizied Prototype and Documentations	30 days	September 18, 2020	October 29, 2020
84	23 Prototype and Documentation Finalized	0 days	October 29, 2020	October 29, 2020
85	24 RPC Link System PRR	0.4 wks	October 30, 2020	November 2, 2020
86	25 Ready for mass Production	0 days	November 2, 2020	November 2, 2020
87	26 Ordering Components	120 days	November 3, 2020	April 19, 2021
88	27 PCB Fabrication	90 days	November 3, 2020	March 8, 2021
89	28 PCB Fabricated and Components Received	0 days	April 20, 2021	April 20, 2021
90	29 PCB Assembly Part-1 (Group 1)	75 days	April 20, 2021	August 2, 2021
91	30 Functional Testing - Part-1 (Group 2)	75 days	August 3, 2021	November 15, 2021
92	31 The First Half of the Link Boards and Control Boards Assembled and Tested	0 days	November 15, 2021	November 15, 2021
93	32 PCB Assembly Part-2 (Group 1)	75 days	August 3, 2021	November 15, 2021
94	33 Functional Testing - Part-2 (Group 2)	75 days	November 16, 2021	February 28, 2022
95	34 The Second Half of the Link Boards and Control Boards Assembled and Tested	0 days	February 28, 2022	February 28, 2022
96	35 Packaging and Integration	30 days	March 1, 2022	April 11, 2022
97	36 Shipment	30 days	April 12, 2022	May 23, 2022



ID	Task Name	Duration	Start	Finish
0	LinkBoard Final Gantt V1-A6_2017_08_03	271.4 wks	March 10, 2017	May 23, 2022
1	1 Analyzing the Legacy SCH & PCBs	10 wks	March 10, 2017	May 18, 2017
2	1.1 LinkBoard	50 days	March 10, 2017	May 18, 2017
3	1.2 Control Board	50 days	March 10, 2017	May 18, 2017
4	2 Analyzing the Legacy FPGA'S Firmware	10 wks	June 2, 2017	August 10, 2017
9	3 Analyzing the Communication Protocol (Reciever/ Transmitter)	100 days	May 19, 2017	October 5, 2017
10	4 FPGA Selection Study	150 days	March 10, 2017	October 5, 2017
11	5 Single Event Upset Study on FPGAs	50 wks	May 19, 2017	May 3, 2018
13	6 Analyzing of ASIC Chips	10 wks	August 11, 2017	October 19, 2017
20	7 Design and Simulation of ASIC Chip IP Cores by FPGAs	10 wks	October 20, 2017	December 28, 2017
27	8 Implementing of ASIC Chip IP Cores in FPGAs	10 wks	December 29, 2017	March 8, 2018
34	9 Hardware Test ot the IP Cores/ Re-Design	10 wks	March 9, 2018	May 17, 2018
41	10 Implementing of IP Cores in FPGAs +SEU	10 wks	May 18, 2018	July 26, 2018
48	11 Hardware Test of IP Cores in FPGAs + SEU with SEU Emulator / Re-Design	10 wks	July 27, 2018	October 4, 2018
55	12 Hardware Test of IP Cores in FPGAs + SEU with Proton Beam/fem Laser/Plasma Focus / Re-Design	10 wks	July 27, 2018	October 4, 2018
62	13 Integration of Cores and Design of Initial Prototype	24 wks	October 5, 2018	March 21, 2019
75	14 Prototype Test of Initial Linkboard/Control Board / Re-Design	40 days	March 22, 2019	May 16, 2019
76	15 Final Prototype Design / Documentation	15 days	May 17, 2019	June 6, 2019
77	16 Final Prototype Design Review / Documentation	15 days	June 7, 2019	June 27, 2019
78	**17 Final Prototype Design Ready**	0 days	June 27, 2019	June 27, 2019
79	18 Initial Validation (Hardware test of the chips +SEU with Proton beam/fem Laser/Plasma Focus/ Re-design)	90 days	June 28, 2019	October 31, 2019
80	**19 Initiale Validation of Final Prototype in IPM**	0 wks	October 31, 2019	October 31, 2019
81	20 Final Validation of Final Prototype Design at CERN	230 days	November 1, 2019	September 17, 2020
82	**21 Final Validation of Final Prototype Design At CERN**	0 days	September 18, 2020	September 18, 2020
83	22 Finalizied Prototype and Documentations	30 days	September 18, 2020	October 29, 2020
84	**23 Prototype and Documentation Finalized**	0 days	October 29, 2020	October 29, 2020
85	24 RPC Link System PRR	0.4 wks	October 30, 2020	November 2, 2020
86	**25 Ready for mass Production**	0 days	November 2, 2020	November 2, 2020
87	26 Ordering Components	120 days	November 3, 2020	April 19, 2021
88	27 PCB Fabrication	90 days	November 3, 2020	March 8, 2021
89	**28 PCB Fabricated and Components Received**	0 days	April 20, 2021	April 20, 2021
90	29 PCB Assembly Part-1 (Group 1)	75 days	April 20, 2021	August 2, 2021
91	30 Functional Testing - Part-1 (Group 2)	75 days	August 3, 2021	November 15, 2021
92	**31 The First Half of the Link Boards and Control Boards Assembled and Tested**	0 days	November 15, 2021	November 15, 2021
93	32 PCB Assembly Part-2 (Group 1)	75 days	August 3, 2021	November 15, 2021
94	33 Functional Testing - Part-2 (Group 2)	75 days	November 16, 2021	February 28, 2022
95	**34 The Second Half of the Link Boards and Control Boards Assembled and Tested**	0 days	February 28, 2022	February 28, 2022
96	35 Packaging and Integration	30 days	March 1, 2022	April 11, 2022
97	36 Shipment	30 days	April 12, 2022	May 23, 2022



Thank you